UTILITY PATENT APPLICATION TRANSMITTAL UNDER 37 C.F.R.§1.53(b)

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Box PATENT APPLICATION
Washington D.C. 20231

Case Docket No.: P-150

Sir:

Transmitted herewith for filing is the patent application of
INVENTOR OR APPLICATION IDENTIFIER: See-Hyun KIM and Hee-Sub LEE
FOR: METHOD FOR DECODING AND DISPLAYING DIGITAL BROADCASTING SIGNALS
Enclosed are:

1. [X] 14 pages of specification, claims, abstract
2. [X] 6 sheets of FORMAL drawing.
3. [X] 2 pages of newly executed Declaration & Power of Attorney (original).
4. [X] Priority Claimed to Korean Appln. No. 51281/1999 and 54741/1999, whose entire disclosures are incorporated herein by reference.
5. [ ] Small Entity Statement.
6. [ ] Information Disclosure Statement, Form PTO-1449 and reference.
7. [X] Assignment Papers for LG Electronics Inc. (cover sheet, assignment & assignment fee).
8. [X] Certified copy of Korean Patent Application No. 51281/1999 filed November 18, 1999 and 54741/1999 filed December 3, 1999.
9. [X] Two (2) return postcards.
   [X] Stamp & Return with Courier.
   [X] Prepaid Postcard-Stamped Filing Date & Returned with Unofficial Serial Number.
10. [X] Authorization under 37 C.F.R. §1.136(a)(3).
11. [ ] Other:

CLAIMS AS FILED					
For	No. Filed		No. Extra	Rate	Fee
Total Claims	14	- 20	0	X $18.00	$0.00
Indep. Claims	1	- 3	0	X $80.00	$0.00
Multiple Dependent Claims (If applicable)				X $270.00	$0.00
				BASIC FEE	$710.00
				TOTAL FILING FEE	$710.00

[ ] This is a Continuation-in-part (CIP) of prior application No: _____ filed _____. Incorporation By Reference-The entire disclosure of the prior application is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

[ ] Amend the specification by inserting before the first line the sentence:
--This application is a continuation-in-part of Application Serial No. _____ filed _____.-

[X] A check in the amount of $710.00 (Check #9773) is attached.

[ ] Please charge my Deposit Account No. 16-0607 in the amount of $__. A duplicate copy of this sheet is enclosed.

[X] The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 16-0607. A duplicate copy is enclosed.
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[X] The Commissioner is hereby authorized to charge payment of following fees during the pendency of this application or credit any overpayment to Deposit Account No. 16-0607. A duplicate copy of this sheet is enclosed.
[X] Any patent application processing fees under 37 C.F.R. 1.17.
[X] Any filing fees under 37 C.F.R. 1.16 for presentation of extra claims.

FLESHNER & KIM, LLP

Daniel Y.J. Kim
Registration No. 36,186

Correspondence Address Below:
P.O. Box 221200
Chantilly, VA 20153-1200
(703) 502-9440 DYK/hmt

Date: November 16, 2000

METHOD FOR DECODING AND DISPLAYING DIGITAL BROADCASTING SIGNALS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for decoding and displaying digital broadcasting signals, in particular to a method for storing the decoded picture for preventing a frame buffer conflict irrespective of location and size of a display window on the screen in decoding and displaying digital broadcasting signals.

2. Description of the Related Art

The digital television (DTV) broadcasting has started in the United States since 1998.. Many efforts have been made to develop DTV sets and set-top boxes for receiving the digital television signal. Recently, an interactive set-top box has been presented, which provides communication services based on the web by displaying a small window on the television screen while a user watches a television program.

However, since the DTV set is quite expensive for general customers, there are much attentions on the development of a low price set-top boxes.

PC (personal computer) add-in cards would be another economical solution for DTV viewing because a PC platform provides a powerful development environment and user interface. Using a local bus or a video signal interface, for

example Video Interface Port (VIP1.1), standard definition (SD) pictures can be transmitted from a DTV reception card to a graphic card. Thus, DTV can be put together with other graphic windows on the monitor.

If the broadcasting videos are HD (High Definition) programs the HD video signals should be outputted to a graphic controller supporting a new video signal interfacing standard such as VIP 2.0. However, it is not easy to transfer the HD video signal to the graphic controller because such a high bandwidth video signal interface such as VIP2.0 is not popular yet and it causes heavy load for a local bus. Therefore, is hard to overlay the HD program within the graphic controller.

Another alternative way to view HD video on the PC monitor is to overlay the video with other graphics in the analog domain. One input of the analog overlay device is the decoded video signal from the DTV reception card and the other input comes from the graphic card with an empty window for DTV video to be displayed. Therefore, user can watch HD programs on a window in the PC monitor.

For digital video broadcasting, Advanced Television System Committee (ATSC) adopts MPEG-2 (Moving Picture Experts Group 2) video compression technology. Using MPEG-2 video compression algorithm, four to six SD programs or one HD program can be transmitted through the channel of the same bandwidth as the National Television System Committee (NTSC) specification.

One technique of MPEG-2 is to exploit a temporal redundancy to compress the video signal. Each frame can be encoded in an intra mode (I-frame), prediction mode (P-frame) or bi-directional prediction mode(B-frame). In order to decode B pictures, it is required to have at least three frame buffers; two for reference frames and one for decoded frame. FIG. 1 is a block diagram illustrating

the general coding and display apparatus with three frame buffers. The apparatus might have more than three frame buffers, but it causes the increase of the material cost. For 1920× 1080 pictures, one frame buffer amounts to 3.1 Mbytes.

As depicted in FIG. 1, the decoder 1 decodes DTV signals and stores the picture data in the buffer memory 2. And, the data stored in the buffer memory 2 is fetched and displayed by the display device 3.

Since there are two buffers for I or P frame, there is no buffer conflict for decoding and displaying I or P pictures simultaneously. That is, when I or P picture is decoded and displayed concurrently, the picture in one I or P buffer is being displayed, the other will be used for storing new picture.

However, there are more than two pictures in a row, say B1 and B2, one B frame buffer has to take care of both decoding and displaying pictures. In other words, B2 picture data can not be stored before B1 data has been fetched, and the fetching operation for B2 can not be performed until B2 data has been stored.

Herein, a covalent process of the B-frame buffer in the data storing and fetching operation will now be described in detail with reference to the accompanying FIG.2 and FIG.3.

First, FIG. 2 illustrates a timing chart for comparing the data storing time and data fetching time when displaying interlaced pictures on a interlace monitor. Also, it is assumed that the size of display window is same as the size of the whole screen.

As depicted in FIG. 2, the decoding and display process are apart by a half frame time. For B pictures, the top field of B1 picture (B1t) is displayed a half frame time after starting to decode the B1 picture, and the B2 picture starts to be decoded when the bottom field of B1 picture (B1b) is displayed.

FIG. 3 is a memory map illustrating the data storing and fetching process for the frame pictures. The top and bottom field data are stored in the order of W1.

When the top field is displayed, the top-field data (top_line(0)~top_line(N-2)) are fetched in the order of R1.R2 denotes the fetch order for displaying the bottom field.

Provided that a picture can be decoded in a frame time, the top field data will be stored before it is displayed and the bottom field data will be fetched before a new picture is stored. Accordingly, when the video is displayed on the whole screen of the monitor, a buffer memory conflict in storing and fetching data does not occur.

However, at a letter box mode of 16:9 pictures on a 4:3 monitor as shown in FIG.4A, or at an analog overlay mode as shown in FIG. 4B,there is a T-gap or B-gap where videos are not displayed on the upper or lower portion of the screen. As the fetching time for display is shortened, the decoding time is affected.

FIG. 5A is a timing chart for illustrating the decoding and display timing when there is T-gap, i.e., the video is not displayed on the upper portion of the screen. As depicted in FIG. 5A, the decoding process for the second B picture (B2) should be delayed until the bottom field of B1 (B1b) starts to be displayed.

In addition, FIG. 5B is a timing chart for illustrating the decoding and display timing when there is B-gap, i.e., the video is not displayed on the lower portion of the screen. As depicted in FIG. 5B, the decoding process should be completed as early as the scanning time of the B-gap.

Consequently, the decoding process should be controlled so that it would not cause a frame buffer memory conflict described above.

In order to prevent the above mentioned frame buffer conflict, one additional buffer memory can be employed for the B picture or a decoder with higher performance can be integrated. But, it causes increase of the manufacturing cost.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method for decoding and storing digital broadcasting signals without an additional buffer memory when there is T-gap where videos are not displayed on the upper portion of a screen.

The other object of the present invention is to provide a method for decoding and storing the digital broadcasting signals which allows the decoder to exploit entire decoding time even with a B-gap where videos are not displayed on the lower portion of the screen.

In order to achieve the above mentioned objects, a method for decoding and storing digital broadcasting signals according to the present invention comprises a process for detecting a non-display section where the videos are not displayed on a display screen, a process for judging whether the non-display section is on the lower portion of the screen, a process for adjusting an edge timing to a display completion timing by shifting a decoding field ID as time as the non-display section when the non-display section is on the lower portion of the screen, and a process for performing the first and the second memory control mode by turns.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram illustrating the general decoding and display apparatus for digital television broadcasting.

Figure2 is a timing chart for illustrating the decoding and display process when the size of a DTV window is same as the size of a whole screen.

Figure 3 is a memory map for a picture, and illustrating the order of storing and fetching scan line data.

Figure 4A illustrates the display of a resized video. Specifically it is a letter box mode of 16:9 pictures on a 4:3 monitor.

Figure 4B illustrates the display of a resized video. Specifically it is a analog overlay mode on a PC monitor.

Figure 5A is a timing chart illustrating the decoding and display process when the video is not displayed on the upper portion of the screen.

Figure 5B is a timing chart illustrating the decoding and display process when the video is not displayed on the lower portion of the screen.

Figure 6A is a memory map illustrating the first memory control mode of the present invention.

Figure 6B is a memory map illustrating the second memory control mode of the present invention.

Figure 7 is a timing chart illustrating the decoding and display process when the timing of the decoding field ID is adjusted.

Figure 8 is a flow chart illustrating how to apply the present invention to exploit entire decoding time.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Hereinafter, the preferred embodiments of the present invention will now be described in more detail.

First, FIG. 6A is a memory map illustrating a first memory control mode of the present invention. The first half data of the first B frame (B1) is stored by skipping over one address (0, 2, 4,..., N-2) from the first address (0) in the order of W2.And the second half data of B1 is stored in the skipped addresses (1, 3, 5, ..., N-1) in the order of W3.

In other words, the data is stored advance on the even addresses (2X, herein X=0, 1, 2, ...) W2, after that, the data is stored on the odd addresses (2X+1, herein X=0, 1, 2, ...) W3.

When the decoded data is stored by the first memory control mode, the top-field data (top_line(0)) is stored on the first address (0), the bottom_field data (bot_line(1)) is stored on the next address (2), and the top-field data (top_line(2)) is stored on the next address (4). Thus, two consecutive field lines, i.e., (top_line(0) and top_line(2) or bot-line(1) and bot_line(3) are located apart by four addresses.

To display the top field of B1, the picture data will be fetched in the order of R3 and R4. Similarly, the bottom field is fetched in the order of R5 and R6. Once the top field has been displayed, the memory for the top field becomes free. So, the decoded data of the second B picture (B2) can be stored in that memory even if the display of the bottom field of B1 has not started.

FIG. 6B is a memory map illustrating a second memory control mode of the present invention. The first half data of the second B frame (B2) is stored in the order of W4 at the addresses of 4x and 4X+1, herein X=0, 1, 2,..., which

become vacant by the fetching processes of the top field data (R3 and R4), which has been stored at the first memory control mode.

The second half data of the second B frame (B2) are stored in the order of W5 at the addresses of 4X+2 and 4X+3, herein x=0, 1, 2, ..., which become vacant by the fetching process of the bottom-field data, R5 and R6.

To display the B2 picture, the data is fetched in the order of R7 and R8 for the top field, R9 and R10 for the bottom field. Once the top field has been displayed, the third B picture can be stored with the first memory control mode .

FIG. 7 is a timing chart illustrating the decoding and display process when the video is not displayed on the lower portion of the screen, so the timing of the decoding field ID is adjusted.

By shifting the decoding field ID as time of "C", the storing completion timing of the data is coincided with the fetching completion timing. . Thus, the loss of the decoding time can be compensated by starting the decoding process as early as B-gap.

FIG. 8 is a flow chart explaining steps for applying the present invention.

First, the non-display section is detected S1, and the section is judged whether it is lower portion of the screen S2.

Herein, when the data is stored and fetched by the first and second memory control mode as depicted in FIG. 6A and FIG. 6B, there is no need to detect and judge whether the non-display section is the upper portion .

According to this, when the videos are not displayed on the lower portion of the screen, the numbers of the scanning line on the non-display lower portion are detected S3.

After that, timing for shifting the edge timing of the decoding filed ID to the

display completion timing is judged by multiplying the numbers of scanning line by the scanning time S4.

After that, the vertical synchronization signal of the decoding field ID is delayed-outputted as the shifting timing S5, and the edge time is adjusted to the display completion time.

Herein, the vertical synchronization signal of the decoding field ID for displaying on the screen in real, it is fixed as hardware-like, accordingly the vertical synchronization signal of the decoding filed ID is adjusted.

After that, when the edge timing adjustment of the decoding field ID is completed, the first and second memory control mode are performed by turns S6.

As described above, according to the present invention, decoded B picture data can be effectively stored. With two different storing schemes, the top and bottom field data can be stored and fetched independently. Thus, by applying two schemes by turns the decoding process does not have to wait for T-gap, even without an additional frame buffer.

As also described above, according to the present invention, the decoder can exploit entire decoding time even with B-gap. By shifting the decoding field ID ahead as much as B-gap, decoding process can be started as early as B-gap. So, the decoding time will not be reduced even if there is B-gap.

The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The teaching of the present invention can be readily applied to other types of apparatuses. The descriptions of the present invention are intended to be illustrative, and not to limit the scope of the claims. Various alternatives, modifications, and variations will be apparent to those skilled in the art.

What is claimed is :

1. A method for decoding and storing digital broadcasting signals, comprising :

detecting a non-display section where broadcasting video is not displayed on a screen ;

judging whether the non-display section is on the lower portion of the screen ;

adjusting an edge timing to a display completion timing by shifting a decoding field ID as time as the non-display section when the videos are not displayed on the lower portion of the screen ; and

performing a first memory control mode and a second memory control mode by turns in order to prevent collisions between the fetching timing of the data to be displayed and the storing timing of the decoding data.

2. The method for decoding and storing digital broadcasting signals according to claim 1, wherein the shift timing of the decoding field ID can be calculated by detecting numbers of scanning line in the non-display section and multiplying it by the scanning time.

3. The method for decoding and storing digital broadcasting signals according to claim 2, wherein the size and position information of the broadcasting video window such as the numbers of scanning line can be gotten easily form an operating system of a PC.

4. The method for decoding and storing digital broadcasting signals according to claim 1, wherein the first memory control mode and the second memory control mode are performed by turns in regardless of the size of the section when the non-display section is on the upper portion.

5. The method for decoding and storing digital broadcasting signals according to claim 1, wherein, when the broadcasting video is not displayed on parts of the upper and lower portions of the screen, the method comprises :

adjusting the edge timing to the display completion time by shifting the decoding field ID as the display time corresponding to the lower non-display portion; and

performing the first and second memory control mode by turns.

6. The method for decoding and storing digital broadcasting signals according to claim 1, wherein the first memory control mode stores orderly the data decoded for the first half cycle of the decoding field ID on the even addresses (2X, herein X=0, 1, 2,...), and stores orderly the data decoded for the next half cycle on the odd addresses (2X+1, herein X=0, 1, 2,...).

7. The method for decoding and storing digital broadcasting signals according to claim 6, wherein the decoded data can be stored on the odd addresses (2X+1, herein x=0, 1, 2,...) first, and later the even addresses (2X, herein X=0, 1, 2,...).

8. The method for decoding and storing digital broadcasting signals

according to claim 1, wherein the second memory control mode stores orderly the data decoded for the first half cycle of the decoding field ID on the addresses (4X, 4X+1, herein X=0, 1, 2,...), and stores orderly the data decoded for the next half cycle on the addresses (4X+2, 4X-3, herein x=0, 1, 2, ...).

9. The method for decoding and storing digital broadcasting signals according to claim 1, wherein difference of four addresses occur on the each consecutive field data stored by the first and second memory control mode.

10. The method for decoding and storing digital broadcasting signals according to claim 1, wherein the top field data fetches the data on the addresses (4X, herein x=0, 1, 2,...), and orderly fetches and displays the data on the addresses (4X+1, herein X=0, 1, 2,...) when the data stored by the first memory control mode are displayed.

11. The method for decoding and storing digital broadcasting signals according to claim 1, wherein the bottom field data fetches the data on the address (4X+2, herein X=0, 1, 2,...) first, and orderly fetches and displays the data on the addresses (4X+3, herein X=0, 1, 2,...) when the data stored by the first memory control mode are displayed.

12. The method for decoding and storing digital broadcasting signals according to claim 1, wherein the top field data fetches the data on the addresses (4X, herein x=0, 1, 2,...), and orderly fetches and displays the data on the addresses (4X+2, herein X=0, 1, 2,...) when the data stored by the second

memory control mode are displayed.

13. The method for decoding and storing digital broadcasting signals according to claim 1, wherein the bottom field data fetches the data on the address (4X+1, herein X=0, 1, 2,...) first, and orderly fetches and displays the data on the addresses (4X+3, herein X=0, 1, 2,...) when the data stored by the second memory control mode are displayed.

14. The method for decoding and storing digital broadcasting signals according to claim 1, wherein the decoding data is the B-frame data.

15. The method for decoding and storing digital broadcasting signals according to claim 14, wherein the process for storing or fetching the B-frame data is performed through the one buffer memory.

ABSTRACT OF THE DISCLOSURE

The present invention relates to a method for decoding and storing digital broadcasting signals which is capable of freely adjusting size and position of a broadcasting video window by preventing a frame buffer conflict between storing and fetching timing of the decoded data which can be occurred depending on the position and the size of the video window displayed on a screen, without expanding memory or upgrading speed of the decoder.

FIG. 1
CONVENTIONAL ART

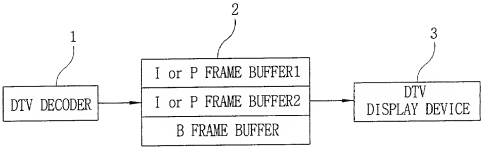


FIG. 2
CONVENTIONAL ART

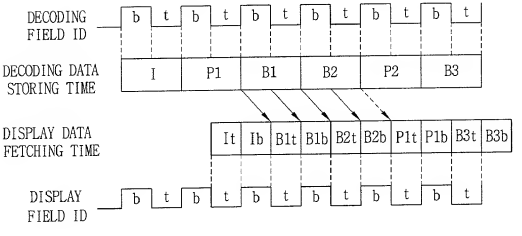


FIG. 3
CONVENTIONAL ART

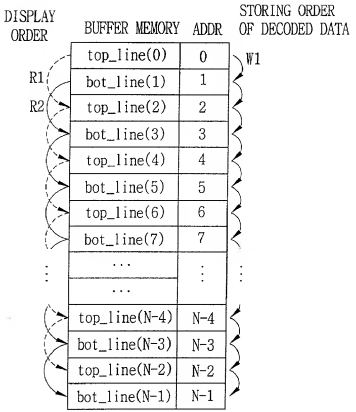


FIG. 4A
CONVENTIONAL ART

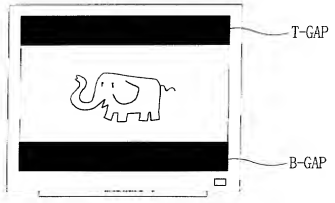


FIG. 4B
CONVENTIONAL ART

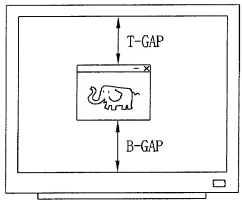


FIG. 5A
CONVENTIONAL ART

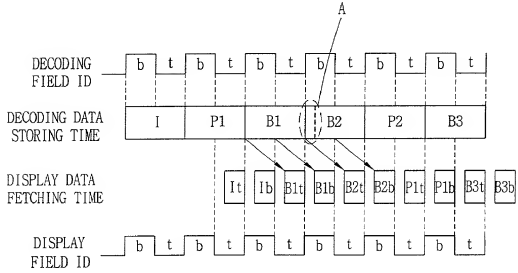


FIG. 5B
CONVENTIONAL ART

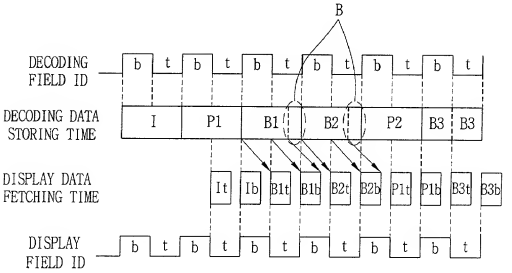


FIG. 6A

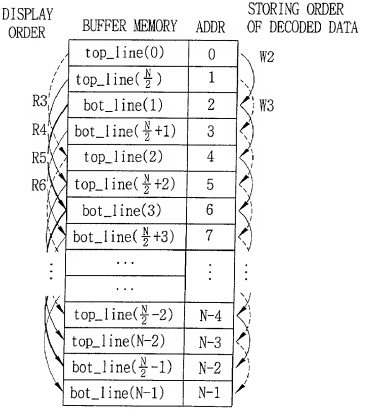


FIG. 6B

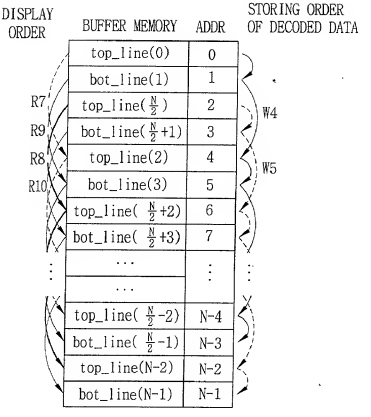

DISPLAY ORDER
BUFFER MEMORY
ADDR
STORING ORDER OF DECODED DATA
top_line(0)
0
bot_line(1)
1
top_line(N/2)
2
bot_line(N/2+1)
3
top_line(2)
4
bot_line(3)
5
top_line(N/2+2)
6
bot_line(N/2+3)
7
top_line(N/2-2)
N-4
bot_line(N/2-1)
N-3
top_line(N-2)
N-2
bot_line(N-1)
N-1
R7
R9
R8
R10
W4
W5

FIG. 7

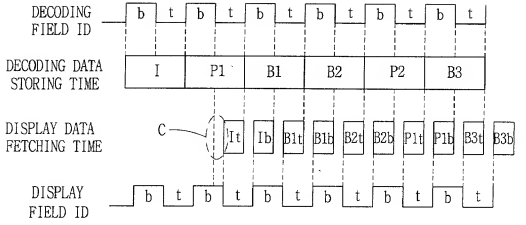
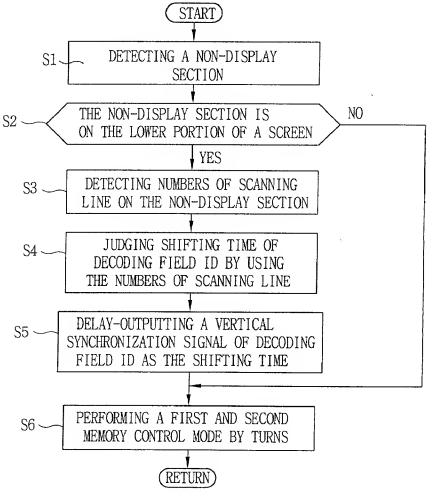

DECODING FIELD ID
b t b t b t b t b t b t
DECODING DATA STORING TIME
I P1 B1 B2 P2 B3
DISPLAY DATA FETCHING TIME
C
It Ib B1t B1b B2t B2b P1t P1b B3t B3b
DISPLAY FIELD ID
b t b t b t b t b t b t

FIG. 8


START
S1
DETECTING A NON-DISPLAY SECTION
S2
THE NON-DISPLAY SECTION IS ON THE LOWER PORTION OF A SCREEN
NO
YES
S3
DETECTING NUMBERS OF SCANNING LINE ON THE NON-DISPLAY SECTION
S4
JUDGING SHIFTING TIME OF DECODING FIELD ID BY USING THE NUMBERS OF SCANNING LINE
S5
DELAY-OUTPUTTING A VERTICAL SYNCHRONIZATION SIGNAL OF DECODING FIELD ID AS THE SHIFTING TIME
S6
PERFORMING A FIRST AND SECOND MEMORY CONTROL MODE BY TURNS
RETURN

Docket No. _____

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought on the invention entitled METHOD FOR DECODING AND DISPLAYING DIGITAL BROADCASTING SIGNALS, the specification of which

[x] is attached hereto [ ] was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is known to me to be material to patentability in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365 (b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s): Number	**Country**	**Foreign Filing Date Month/Day/Year**
51281/1999	Korea	11/18/1999
54741/1999	Korea	12/3/1999

hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s):	**Filing Date (Month/Day/Year)**

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Prior U. S. Application or PCT Parent Number	**Filing Date (Month/Day/Year)**	**Parent Patent Number (if applicable)**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) and/or agent(s):Daniel Y.J. Kim, Registration No. 36,186 and Mark L. Fleshner, Registration No. 34,596; Carl R. Wesolowski, Registration No. 40,372, John C. Eisenhart, Registration No. 38,128, Rene A. Vazquez, Registration No. 38,647; Michael J. Cornelison, Registration No. 40,395; and Stuart I. Smith, Registration No. 42,159; and Carol L. Druzbick, Registration No. 40,287, all of

FLESHNER & KIM
P. O. Box 221200
Chantilly, Virginia 20153-1200

with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and all future correspondence should be addressed to them.

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Full name of sole or first inventor: See-Hyun KIM

Inventor's signature: Seehyun Kim Date: NOV. 9, 2000

Residence: Republic of Korea

Citizenship: Yongin Korea

Post Office Address: Daejin 2 Cha Apt. 103-1501, 883-1, Jukjeon-Ri, Suji-Eub, Yongin, Kyunggi-Do, Korea

****

Full name of joint inventor(s): Hee-Sub LEE

Inventor's signature: Date: NOV. 9, 2000

Residence: Republic of Korea

Citizenship: Kwacheon Korea

Post Office Address: Jukong Apt. 1017-102, 67, Jungang-Dong, Kwacheon, Kyunggi-Do, Korea

****

Full name of joint inventor(s):

Inventor's signature: Date:

Residence:

Citizenship:

Post Office Address: